

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-5 (Canceled)

Claim 6 (Previously Presented) A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate by a thermal oxide film;

forming a gate electrode pattern on said gate oxide film;

forming diffusion regions in said substrate at both lateral sides of said gate electrode pattern by introducing an impurity element into said substrate through said gate oxide film while using said gate electrode pattern as a mask; and

introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask,

said step of introducing said impurity element being conducted prior to said step of introducing N atoms into said gate oxide film,

wherein said step of introducing N atoms into said gate oxide film comprises a

thermal annealing process of said gate oxide film conducted in an atmosphere containing NO,
wherein activation of said impurity element is conducted simultaneously to said
thermal annealing process,
said thermal annealing process being conducted at a temperature of about 800°C.

Claims 7-9 (Canceled)

Claim 10 (Previously Presented) A method of fabricating a semiconductor device,
comprising the steps of:
 forming a gate oxide film on a substrate by a thermal oxide film;
 forming a gate electrode pattern on said gate oxide film such that said gate
 electrode pattern is in direct contact with said oxide film;
 forming diffusion regions in said substrate at both lateral sides of said gate
 electrode pattern by introducing impurity element into said substrate through said gate oxide film
 while using said gate electrode pattern as a mask; and
 introducing N atoms, after said step of introducing said impurity element, into said
 gate oxide film while using said gate electrode pattern as a mask, such that said N atoms do not
 reach said substrate,
 wherein said step of introducing N atoms into said gate oxide film includes an ion

U.S. Patent Application Serial No. 09/428,052

implantation process of N ions conducted under an acceleration voltage not exceeding 10keV, with a dose of $1 - 3 \times 10^{14} \text{ cm}^{-2}$.

Claims 11-14 (Canceled)

Claim 15 (Previously Presented) A method of fabricating a semiconductor device, comprising the steps of :

forming a gate oxide film on a substrate;
forming a gate electrode pattern on said gate oxide film; and
introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask, said step of introducing N atoms being conducted in an atmosphere containing NO; and

depositing, after said step of introducing N atoms, a CVD-oxide film on said gate oxide film by a CVD process,

wherein said step of introducing N atoms and said step of depositing said CVD-oxide film are conducted consecutively in a common processing chamber, without taking out said substrate into an atmospheric environment.

Claim 16 (Previously Presented) A method as claimed in claim 15, further comprising the step of forming diffusion regions at both lateral sides of said gate electrode pattern by introducing impurity elements into said substrate through said gate oxide film while using said gate electrode pattern as a mask, and wherein said step of introducing impurity elements is conducted prior to said step of introducing N atoms into said gate oxide film.

Claim 17 (New) The method as claimed in claim 10, wherein said ion implantation process is conducted such that N ions are introduced perpendicularly to said gate oxide film.

Claim 18 (New) The method as claimed in claim 10, wherein said N atoms are incorporated into said gate oxide film with a concentration of 0.5 - 3%.